FIG. **15** illustrates the single epitaxy step of the method of the invention during which raised source and drain regions are produced.

FIG. **16**A presents an undesired case of a form of spacer foot that is found after etching the layer of silicon nitride according to existing techniques.

FIG. **16**B shows another undesired case where the layer serving for the epitaxial growth of the source and drain is attacked.

FIG. **17** illustrates the absence of the defects mentioned in the previous two figures when the method of the invention is used

The accompanying drawings are given by way of examples and are not limitative of the invention. These drawings are schematic representations and are not necessarily to the scale of the practical application. In particular, the relative thicknesses of the layers and substrates do not represent reality.

DETAILED DESCRIPTION OF THE INVENTION

Before going into the detail of the embodiment of the invention, in particular with reference to the drawings, non-limitative features that the invention may have individually or according to all combinations are briefly introduced below:

the formation of the superficial layer comprises a modification to the material of only part of the thickness of the dielectric layer;

the modification is an oxidation;

the oxidation is carried out conformingly at the flanks and the peripheral region;

the oxidation is carried out using a plasma;

an oxygen plasma is used in which the energy of the ions is between 8 and 13 eV, preferable 10 eV;

the formation of the superficial layer comprises a deposition of a layer of material above the dielectric layer;

the material of the layer of material above the dielectric layer is chosen from a material comprising carbon, an oxide such as silicon dioxide (SiO_2), a material containing germanium and in particular silicon-germanium or a silicon-germanium nitride, preferably a proportion of germanium from 15% to 40%;

the partial removal of this superficial layer is an etching carried out using a plasma;

the etching of the partial removal of the superficial layer is an anisotropic action configured so as to attack the superficial layer at the peripheral region while not attacking the superficial layer at the gate or attacking it less;

the anisotropic etching is carried out with an argon or carbon tetrafluoride plasma in which the energy of the ions is between 8 and 13 eV, preferably 10 eV;

the selective etching is carried out using a plasma;

the anisotropic etching and then the selective etching are carried out in the same reactor;

the selective etching is carried out by wet method

the selective etching is configured so as to partially attack the dielectric layer in a gate foot region situated below the residual part in the direction of the flank of the gate so as to form a recess;

the recess has a height of between 5 and 30 nm, preferably between 10 and 15 nm;

the recess has a width of between 5 and 10 nm and/or a width less than the height of the recess;

the selective etching is configured so as to form a straight edge in the dielectric layer along the thickness of the dielectric layer in alignment with the residual part;

the dielectric layer is made by a layer of nitride, preferably a silicon nitride;

the dielectric layer is made from a low-k material with a dielectric constant lower than that of silicon nitride;

a superficial layer of a fully depleted silicon on insulator (FD-SOI) wafer is used as a semiconductor layer.

In the context of the present invention, the terms "on", "surmounts" or "underlying" or their equivalents do not necessarily mean "in contact with". Thus, for example, the deposition of a first layer on a second layer does not necessarily mean that the two layers are directly in contact with each other but means that the first layer at least partially covers the second layer while being either directly in contact therewith or being separated from it by another layer or another element.

In the following description, the thicknesses are generally measured in directions perpendicular to the plane of the bottom face of the layer to be etched or of a substrate on which the bottom layer is disposed. Thus the thicknesses are generally taken in a vertical direction on the figures depicted. On the other hand, the thickness of a layer covering a flank of a pattern is taken in a direction perpendicular to this flank.

Hereinafter, selective etching means the removal by etching of a given material while at least partially preserving, through the selectivity of the method used, other materials.

The words "superficial layer" means a layer that is formed, in particular, by modifying the underlying layer or by a deposition of this underlying layer on the surface of the electronic device after the formation of the underlying layer. It is next partially removed in order to partly remove the underlying layer. The adjective "superficial" does not necessarily signify that the residual superficial layer always remains on the surface of the device when the manufacture of the latter is finalised. It may for example be removed or covered.

"Conforming" means a layer geometry that has the same thickness, to within the manufacturing tolerances, an identical thickness despite the changes in direction of the layer, for example despite the changes in direction of the layer, for example at the gate pattern flanks.

The word "dielectric" means material the electrical conductivity of which is sufficiently low in the given application to serve as an insulator.

The method for producing spacers according to the invention is illustrated by FIGS. **9** to **14**. The method applies after the gates of the transistors have been formed, that is to say from a structure such as that illustrated by FIG. **8**, which is not different, in this example, from that of FIG. **1** already described. The method of the invention can in fact potentially be implemented from any MOSFET transistor structure after the gate patterns have been defined by photolithography.

In FIG. **8**, used as a typical example of a starting point for an application of the method of the invention, the elements already described are therefore found:

The source and drain regions **220** and **221**, which are overall designated as source/drain regions since they are very generally perfectly symmetrical and can fulfil one or other role according to the electrical biasings that are applied to the transistor.

The gate **200** conventionally consists of a stack of layers, a major part of which always consists of polycrystalline silicon **201**. The layers **203** and **204** constitute the gate oxide